REMARKS

Claims 1-16 and 18 are pending in the application, with claims 1-15 having been withdrawn from consideration. The applicants respectfully submit that no new matter has been added. It is believed that this Amendment is fully responsive to the Office Action dated **May 2, 2003**.

IDS

On October 1, 2002 an IDS was filed in this application. The applicant has yet to receive the signed 1449 form. Therefore, the Examiner is requested to return the PTO-1449 form in response to this request for reconsideration.

Assertion of Product by Process Claims

In item 4 of the office action it is asserted that claims 16 and 18 are product by process claims. This assertion is respectfully traversed. Both claim 16 and 18 further detail the structure of the present invention and not how it is made. As provided in claim 16, the structure of the first and third gate electrodes is further detailed. Therefore, withdrawal of the assertion that claims 16 and 18 are directed to product by process claims is respectfully requested.

Claim Rejections under 35 USC §103

Claims 16 and 18 are rejected under 35 USC §103(a) as being unpatentable over admitted Prior Art Figure 8 and Gwen et al. (U.S. Patent No. 5,472,892).

Figure 8 describes an integrated circuit in the prior art having a flash memory (A), a low voltage transistor (B), and mid-level voltage transistor (D), and a high voltage transistor (C). A semiconductor substrate is used as the base for each of the foregoing devices. In addition, insulation (12B) is shown with a thickness of 1.5-5 nm, insulation (12D) is shown with a thickness of 5-10 nm, and insulation (12C) has a thickness of 8-50 nm. In addition, gate electrode (16), as solely illustrated by figure 8J, appears to illustrate electrodes 16 of equal height. A floating gate (13) with a control gate (16) is formed on the silicon gate (13) using an ONO film (14), as shown in figure 8B. It should also be noted that silicon gate (13) is also referred to as a floating gate (13) in the discussion of figure 17.

Gwen et al. describes the method of the manufacturing gate memory in which a silicon layer (206) is placed in a cell array region and a silicon layer (208) is placed in a peripheral circuit region. According to figure 3I, silicon layer (208) appears to be placed directly upon silicon layer (206).

Gwen et al. does not disclose or suggest a second gate electrode having a second silicon film stacked upon a third silicon film. However, the Examiner asserts that forming a second gate electrode having a second silicon film stacked upon a third silicon film is simply a method of manufacture of the structure and not to be given patentable weight. The Examiner's assertions are respectfully traversed. The stacking of a second silicon film upon a third silicon film is an important part of the structure of the second gate electrode.

Thus, Gwen is silent about the feature of the second silicon film stacked on the third silicon film in the second gate electrode. This feature cannot be derived even when Gwen is combined with Admitted Prior Art.

Further, it is noted that the gate electrode of the peripheral transistor of Gwen has the same layered structure as that of the flash memory cell. Thus, the device of Gwen, using the same stacked gate structure for both the flash memory cell and the peripheral transistor, assumes the use of the same oxide film for both the tunneling film of the flash memory cell and the gate electrode of the peripheral transistor. There is no possibility in Gwen to change the thickness of the gate insulation film for different peripheral transistors designed for different operational voltages. In order to do so, it is necessary to remove the stacked gate structure from the peripheral transistor, while such a procedure is contradictory to the construction of Gwen as shown in FIGS. 3I and 3J.

Thus, the teaching of Gwen is incompatible with the present invention and also incompatible with the device of the Admitted Prior Art (APA). The rejection under 35 U.S.C. 103 (a) thus cannot hold.

The Examiner is continuously arguing that the feature of forming a second gate electrode having a second silicon film stacked upon a third silicon film is simply a method of manufacture of the structure and not to be given patentable weight.

Contrary to the assertion of the Examiner, the construction of the second gate electrode as set forth in claim 16 is an important point for realizing substantially same height for the first through third electrodes. Because the gate electrodes have substantially the same height, the patterning of the gate electrodes can be conducted for the first through third MOS transistors simultaneously by using the same resist pattern 111G as represented in FIG.46L. Further,

formation of contact holes for exposing the gate electrodes can be conducted simultaneously in a single step.

Further, the existence of the silicon layer 13 underneath the silicon layer 16 in the second MOS transistor eliminates the problem of formation of the deep groove at the peripheral part of the device region. Reference should be made to the step of FIG. 46I.

Specifically, independent claims 16 patentably distinguishes over the prior art relied upon, by reciting,

> "A semiconductor integrated circuit, comprising: a semiconductor substrate; a non-volatile memory formed in a memory cell region of said semiconductor substrate; a first MOS transistor formed on a first device region of said semiconductor substrate, said first MOS transistor having a first gate insulation film of first thickness and a first gate electrode; a second MOS transistor formed on a second device region of said semiconductor substrate, said second MOS transistor having a second gate oxide film of second thickness and a second gate electrode; and a third MOS transistor formed on a third device region of said semiconductor substrate, said third MOS transistor having a third gate insulation film of third thickness and a third gate electrode; said first thickness being smaller than said second thickness, said second thickness being smaller than said third thickness, said first through third gate electrodes having a substantially identical height, wherein said first and third gate electrodes have a structure in which a second silicon film is stacked on a first silicon film, said second gate electrode has a structure in which said second silicon film is stacked on a third silicon film, and wherein said non-volatile memory is formed of a floating gate electrode formed of said third silicon film and a control gate electrode formed on said floating gate electrode via an insulation film and having a structure in which said first silicon film and said second silicon film are consecutively stacked." (Emphasis Added)

Therefore, withdrawal of the rejection of Claims 16 and 18 under 35 USC §103(a) as being unpatentable over admitted Prior Art Figure 8 and Gwen et al. (U.S. Patent No. 5,472,892) is respectfully requested.

Conclusion

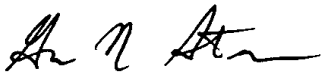
In view of the aforementioned amendments and accompanying remarks, claims, as amended, are in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicants undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

ARMSTRONG, WESTERMAN & HATTORI, LLP



George N. Stevens
Attorney for Applicant
Reg. No. 36,938

GNS/anp/plb
Atty. Docket No. **011225**
Suite 1000
1725 K Street, N.W.
Washington, D.C. 20006
(202) 659-2930

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